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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,550	06/27/2003	Edward A. Burton	INTEL-021	7414

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EXAMINER	
TRAN, LONG K	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/607,550	BURTON ET AL.	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,29 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,6,8,9,10,13,29 and 30* is/are rejected.

7)☒ Claim(s) *2,3,7,11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election without traverse of **Group I**, claims **1 – 14, 29** (typo error in the response: should be **29** not **20**) and **30** in the reply filed on December 06, 2004 is acknowledged.

Drawings

2. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: Brief Description Of The Drawings, [5], line 4 and line 6, add -- Prior Art -- at the end of the paragraphs.

Appropriate correction is required.

Claim Objections

4. Claim 1 is objected to because of the following informalities: the examiner is not clear that the signal wires in each layer are parallel to each other or the signal wires in first layer are parallel to the signal wires in the second layer? For clarification, the

examiner suggests in claim 1, line 4: change " wherein the signal wires in the first and second layers are substantially parallel with each other" --wherein the signal wires in the first layer are substantially parallel to the signal wires in the second layer -- . Clarification is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims **1, 6, 8, 9, 10, 13, 14, 29** and **30** are rejected under 35 U.S.C. 102(e) as being anticipated by Otsuka et al. (US Patent 6,476,330).

7. Regarding claim **1**, Otsuka et al. disclose a semiconductor device comprising:

A first layer (not shown same as 35 (fig. 4)) having a plurality of signal wires 75 (fig. 8), a second layer (not shown same as 38 (fig. 4)) adjacent to the first layer having a plurality of signal wires 76 (fig. 8), wherein the signal wires in the first and second layers are substantially parallel with each other (column 9, lines 45 – 47).

Regarding claim **6**, Otsuka et al. disclose at least one additional layer adjacent to the first and second layer (not shown same as 35 (fig. 4)), wherein signal wires 77 (fig. 8) in the at least one additional layer are substantially parallel to signal wires in the first and second layers.

Regarding claim **8**, Otsuka et al. disclose the semiconductor device comprising: N layers, wherein N is greater than two and wherein the first and second layers are any adjacent layers in the N layers (fig. 8).

Regarding claim **9**, Otsuka et al. disclose the semiconductor device is a microprocessor (column 1, lines 6 – 15).

Regarding claim **10**, Otsuka et al. disclose the first layer and second layer have similar process parameters (column 11, lines 25+).

Regarding claim **13**, Otsuka et al. disclose additional signal wires in the second layer that are located substantially orthogonal to the plurality of signal wires in the first layer (note: column 11, lines31 – 34: the first and second signal wires can run in any direction. Therefore they can run parallel or orthogonally).

Regarding claim **14**, Otsuka et al. disclose the plurality of signal wires in the first layer is a set of related signal wires and wherein the plurality of signal wires in the second layer is a replication of the plurality of signal wires in the first layer (fig. 8).

8. Regarding claim **29**, Otsuka et al. disclose a system comprising a microprocessor; and off-die component in comminication with the microprocessor; wherein the microprocessor (column 1; 5 +) comprising:

A first layer (not shown same as 35 (fig. 4)) having a plurality of signal wires 75 (fig. 8), a second layer (not shown same as 38 (fig. 4)) adjacent to the first layer having a plurality of signal wires 76 (fig. 8), wherein the signal wires in the first and second layers are substantially parallel with each other (column 9, lines 45 – 47).

Regarding claim **30**, Otsuka et al. disclose at least one additional layer adjacent to the first and second layer (not shown same as 35 (fig. 4)), wherein signal wires 77 (fig. 8) in the at least one additional layer are substantially parallel to signal wires in the first and second layers.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims **4** and **5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Otsuka et al. (US Patent 6,476,330) in view of Schaper (US Patent No. 6,388,200).

11. Regarding claim **4**, Otsuka et al. disclose the claimed invention of claim 1 except for a power supply and ground wires are located in both the first layer and the second layer as cited in present claim.

How ever, Schaper shows in figure 1 that power connection 26 in layer 15 and power pad 21 in layer 17; ground pad 20 in layer 17 and ground connection 24 in layer 15.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the signal wire layers of Otsuka et al. with the signal wires layers of Shaper, in order to interconnect different signal wires to the power and ground source in a four metal layer structure.

Regarding claim **5**, figure 1 of Schaper illustrates power supply and ground wires are located in the same respective position in each layer.

Allowable Subject Matter

12. Claims **2, 3, 7, 11** and **12** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is an examiner's statement of reasons for the indication of allowable subject matter: Claims **2, 3, 7, 11** and **12** are allowable over the prior art of record because none of the prior art whether taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach:

Adjacent signal wires are located alternating pattern in the first and second layers (figs. 4, 5(A) – 5 (D)) as cited in claims 2 and 7.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Tran

January 25, 2005

David Nelms
Supervisory Patent Examiner
Technology Center 2800